

28nm CPI (Chip/Package Interactio &

28nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages

*Kang Chen, Linda Chua, Won Kyung Choi, Seng Guan Chow and Seung Wook Yoon**

STATS ChipPAC Pte. Ltd. 5 Yishun Street 23, Singapore 768442

*STATS ChipPAC Pte Ltd. 10 Ang Mo Kio Street 65 Techpoint #04-08/09 Singapore 569059

seungwook.yoon@statschippac.com

Abstract— To meet the continued demand for form factor reduction and functional integration of electronic devices, Wafer Level Packaging (WLP) is an attractive packaging solution with many advantages in comparison with standard Ball Grid Array (BGA) packages. The advancement of fan-out WLP has made it a more promising solution as compared with fan-in WLP, because it can offer greater flexibility in enabling more IO's, multi-chips, heterogeneous integration and 3D SiP. In particular, Embedded Wafer Level BGA (eWLB) is a fan-out WLP solution which can enable applications that require higher input/output (I/O) density, smaller form factor, excellent heat dissipation, and thin package profile, and it has the potential to evolve in various configurations with proven integration flexibility, process robustness, manufacturing capacity and production yield. It also provides integration of multiple dies vertically and horizontally in a single package without substrates.

For eWLB fan-out WLP, the structural design as well as selection of materials is very important in determining the process yield and long term reliability. Therefore it is necessary to investigate the key design factors affecting the reliability comprehensively. Th

based on these finite element analysis (FEA) simulation results, the BEOL stack with the highest CPI risk is chosen for package reliability testing using the CPI test vehicle (TV).

In this work, we assess production readiness for large body size multilayer RDL based eWLB packages through;

- Functional test of 28nm circuits
- Reliability test
- Electrical and thermal characterization
- Thermo-mechanical characterization and simulation

Advanced Wafer-Level Technology: eWLB/FOWLP

eWLB package technology is based on an embedded device technology with fan-out redistribution. The thin-film redistribution layer (RDL) of the eWLB enables very flexible and highly customizable package designs. The length of the redistribution lines is in the range of the die size[5].

eWLB has the ability to attain minimum interconnection length and excellent electrical performance. In a few cases, eWLB achieved a 20~40% reduction in package size a over 50% volume reduction as compared to other packaging solutions such as flipchip or wirebonding packages due its slim and smaller form factor. For radio frequency (R and high-frequency microwave or mmWave devices, significantly improvements in overall device performance was illustrated by eWLB, which showed less parasitic electrical interference.



Figure 2. Key features of advanced eWLB/FO-WI
Innovative and high performance solution of integration

II. EXPERIMENTAL WORKS

Test Vehicle Specification

The three different test vehicles were designed with 10x10-15x15mm package sizes and multi-layer RDL. All those test vehicles were assembled and packaged with 1

Reliab

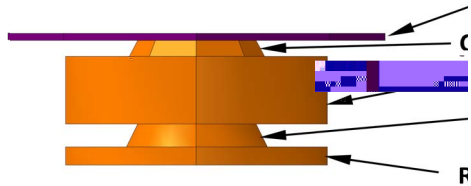
For component level reliabi
were assembled with daisyc
devices. Table 2 shows the
conditions in this study.
All tested eWLB parts testec
package level and board
successfully. eWLB with
passed JEDEC TC-B conditio
cycling (TC) reliability test.
body thickness, it passed 100
300 drops, no failure has
performance was robust

Table 2. Package & Board
eWLB with advanc

Test	
PC Pre-Cond	
TC Temp. Cycling	
HTSL, High Temp Storage Life	
THS, Temp Humidity Storage	
TCoB	
Drop Test	

RDL Via Shap

RDL via shap
advanced node
adopted to ex
interconnect st
BEOL layer in
4 shows a RD
different RDL
tapered via, wl
Other variatio
and 4 are for ;
and a thick Cu
a thin Cu pillar
of the FEA mc
250°C to -55°
normalized ma
different via s
conditions are c



Option 4: Via with Thin Cu Column

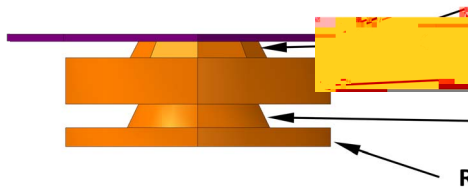


Figure 5. Design options of RDL via interconnection structure

Table 3. Normalized Max. Principal Stress.

Temperature (°C)	Design Option		
	1	2	3
250	1.00	0.91	
125	1.00	0.93	
25	1.00	0.88	
-55	1.00	0.92	

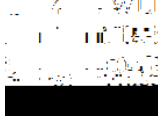
Thermal Characterization

For thermal characterization, the test vehicle was prepared with thermal die having thermal block. Test vehicle specification was as shown in Table 2(b). The effect of die thickness on thermal performance was investigated with 3 different die thicknesses: 100µm, 200µm, and 400µm. For the comparison study, standard flip chip package were prepared.

To easily detect the temperature at the die with applied power, all test vehicles were equipped with a transistor and heating circuit block and a temperature sensor. After surface mount test vehicle was mounted on a JEDEC standard 8-layer thermal test board (PCB), 2.0W power was applied. The temperature was measured with three different die thicknesses. As evident in Fig. 6, there is a significant improvement in thermal performance for the 400µm thickness as compared to flipchip package. This means that we can use a die that is thicker than flipchip package, achieving a more than 25% improvement in thermal performance.

In this work, main findings

- 1. High-match
- 2. Trace
- 3. Trace and 5



Using computer simulation electromagnetic field solver, eWLB and flipchip packages HFSS software, the S-parameters were extracted. Table 4 illustrates the comparison of the results with RLC parameters. For eWLB, it was found that the inductance and resistance were shorter without bump compared with previous results.

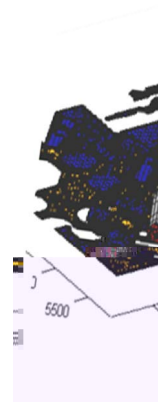


Figure 7. 3D electromagnetic field simulation

Table 4. Comparison of S-parameters

Net	Inductance
	flipchip
1	1.77
2	2.03
3	1.51
4	1.08

